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Packaged Ga_2O_3 Schottky Rectifiers with Over 60 A Surge Current Capability

Ming Xiao, Boyan Wang, Jingcun Liu, *Student Member, IEEE*, Ruizhe Zhang, *Student Member, IEEE*, Zichen Zhang, Chao Ding, Shengchang Lu, Kohei Sasaki, Guo-Quan Lu, *Fellow, IEEE*, Cyril Buttay, *Senior Member, IEEE*, and Yuhao Zhang, *Member, IEEE*

***Abstract* – Ultra-wide-bandgap gallium oxide (Ga_2O_3) devices have recently emerged as promising candidates for power electronics; however, the low thermal conductivity (k_T) of Ga_2O_3 causes serious concerns about their electrothermal ruggedness. This work presents the first experimental demonstrations of large-area Ga_2O_3 Schottky barrier diodes (SBDs) packaged in the bottom-side-cooling and double-side-cooling configurations, and for the first time, characterizes the surge current capabilities of these packaged Ga_2O_3 SBDs. Contrary to popular belief, Ga_2O_3 SBDs with proper packaging show high surge current capabilities. The double-side-cooled Ga_2O_3 SBDs with a 3×3 mm^2 Schottky contact area can sustain a peak surge current over 60 A, with a ratio between the peak surge current and the rated current superior to that of similarly-rated commercial SiC SBDs. The key enabling mechanisms for this high surge current are the small temperature dependence of on-resistance, which strongly reduces the thermal runaway, and the double-side-cooled packaging, in which the heat is extracted directly from the Schottky junction and does need to go through the low-k_T bulk Ga_2O_3 chip. These results remove some crucial concerns regarding the electrothermal ruggedness of Ga_2O_3 power devices and manifest the significance of their die-level thermal management.[1]**

***Index Term* – ultra-wide bandgap, gallium oxide, surge current, ruggedness, package, thermal management, simulation**

I. Introduction

Ultra-wide-bandgap (UWBG) semiconductor gallium oxide (Ga_2O_3) is a promising material for next-generation power electronics due to its high critical electrical field (E_C), controllable doping, excellent thermal stability, and the availability of large-diameter wafers by the melt growth [1], [2]. Recently, kilovolt-class Ga_2O_3 Schottky barrier diodes (SBDs) [3], [4] and power FinFETs [5], [6] were demonstrated with a peak electric field (E-field) in Ga_2O_3, exceeding the E_C of GaN and SiC. However, most of the reported Ga_2O_3 devices have a small current, and only a few large-area Ga_2O_3 devices have been demonstrated with a current over 1 Amp [7], [8].

A fundamental challenge for the current scaling in Ga_2O_3 devices is the low thermal conductivity (k_T) of Ga_2O_3 (0.1-0.3 $Wcm^{-1}K^{-1}$ [1]), which is about 1/6 of the k_T of Si, 1/10 of GaN, and 1/20 of SiC. The high thermal resistance of the Ga_2O_3 die makes its thermal management very challenging. While some modeling and simulation works have investigated the thermal management of Ga_2O_3 devices [9]–[12], no experimental demonstrations of the packaging and thermal management of large-area Ga_2O_3 devices have been reported to date.

Due to the low k_T of Ga_2O_3, Ga_2O_3 devices are often perceived to have very limited electrothermal ruggedness. Surge current ruggedness is essential for power applications, when the device needs to temporarily sustain a current higher than the rated one. The surge current value is listed in a diode's datasheet and is usually measured in a half-sinusoidal current-pulse according to JEDEC standards [13]. While the surge current ruggedness has been extensively studied for SiC diodes [14], [15], no such tests have been reported for Ga_2O_3 devices.

This work presents the first experimental study on the surge current capability of large-area, packaged Ga_2O_3 devices. Vertical Ga_2O_3 SBDs were fabricated with a current over 10 A. Two packaging structures were designed and prototyped, one based on the bottom-side-cooling scheme where the heat must diffuse through the entire Ga_2O_3 chip before reaching the baseplate (Fig. 1(a)), and the other based on the double-side-cooling scheme (Fig. 1(b)), which allows the heat dissipation through the Ga_2O_3 chip and directly from the Schottky junction simultaneously. Despite the low k_T of Ga_2O_3, the double-side-cooled Ga_2O_3 chip showed a high surge current capability over 60 A. The electrothermal dynamics in the packaged Ga_2O_3 SBDs were also studied using mixed-mode simulations.

II. Device Fabrication, Packaging, and Test Setup

The Ga_2O_3 wafer consists of a 10-µm Si-doped n-Ga_2O_3 layer (net donor concentration ~2×10^{16} cm^{-3}) grown on a 2-inch n^+-Ga_2O_3 (001) substrate (Sn: 1.3×10^{19} cm^{-3}). The substrate was thinned down to a thickness of 500 µm. The device fabrication is similar to those reported in [3], [16]. A Ti/Au (30/150 nm) Ohmic contact was formed as the cathode. 1-µm-thick SiO_2 was

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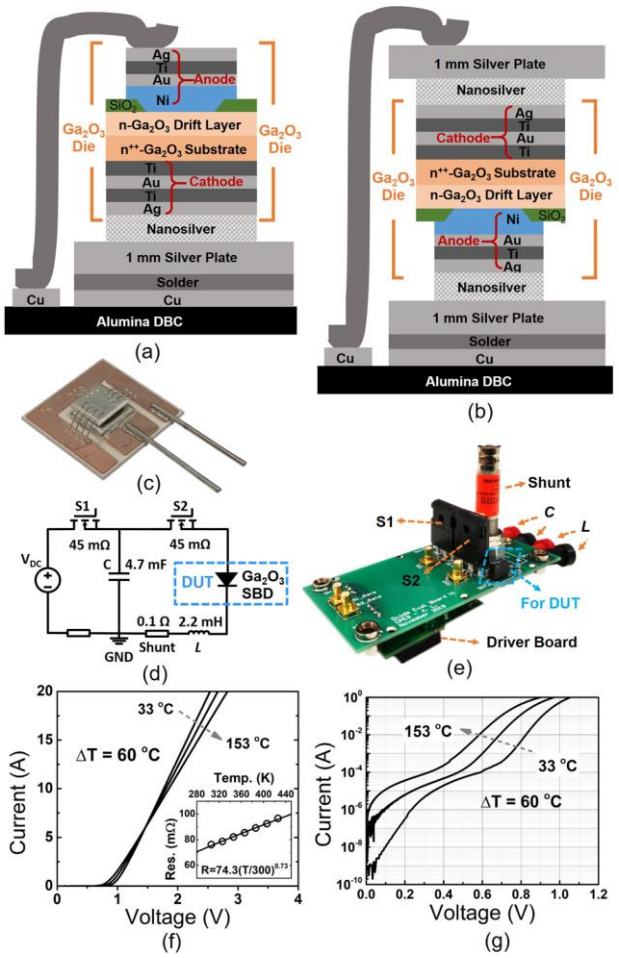


Fig. 1. Schematic of the Ga_2O_3 SBDs with (a) bottom-side-cooling package and (b) double-side-cooling package. (c) Photo of a double-side-packaged SBD. (d) Circuit diagram and (e) photo of the surge current test board. Forward I-V characteristics of the packaged Ga_2O_3 SBDs at 33-153 °C in the (f) linear region and (g) subthreshold region. [inset of (f)] temperature-dependence of the differential R_{on} and the power law fitting.

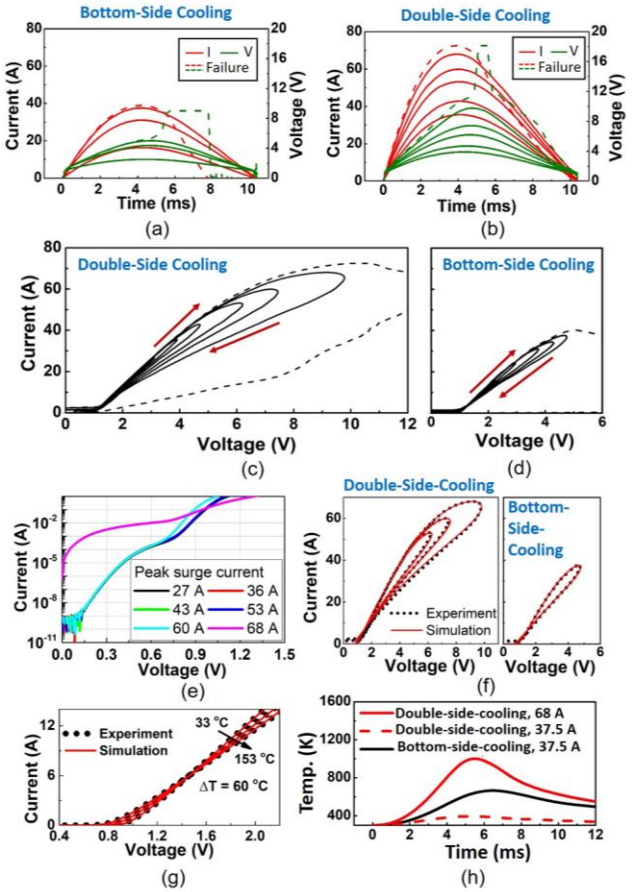


Fig. 2. Current/voltage waveforms of the (a) bottom-side-cooled and (b) double-side-cooled Ga_2O_3 SBDs in the surge current tests. I-V loops of the (c) double-side-cooled and (d) bottom-side-cooled devices. (e) Transfer characteristics in the subthreshold region after each surge current test. Simulation model calibration for the (f) surge I-V loops and (g) static I-V characteristics. (h) Simulated junction temperature in the surge current tests for bottom-side-cooled and double-side-cooled Ga_2O_3 SBDs.

deposited as the field-plate (FP) dielectrics, followed by a wet etch to produce a ~15° FP bevel angle. An Ni/Au stack was deposited as the Schottky and FP metals. 100-nm Ti and 200-nm Ag were deposited on both sides as the contact layer for the device packaging that followed. The Schottky contact area is 3×3 mm^2, and the total sample size is about 4.5×4.5 mm^2.

A nanosilver paste from NBE Technologies was used for the die attach by a pressureless sintering process in air [17], [18]. The sintered-silver joint has a high melting temperature of 960 °C and a high thermal conductivity over 1 $Wcm^{-1}K^{-1}$. A laser-cut mask was used to stencil-print a 50-μm thick nanosilver paste on bonding pads with minimal lateral seepage. The sintering profile was: from room temperature to 250 °C at a ramp rate of 6 °C/min and held at 250 °C for 30 minutes, followed by air cool to room temperature. For the single-side-cooled package, the cathode of the Ga_2O_3 chip was sintered on a 1-mm thick Ag plate, and wire-bonds were attached on the top anode. For the double-side-cooled package, each terminal of the Ga_2O_3 chip was sintered on a 1-mm thick Ag plate. The packaged chips were then soldered on an alumina direct-bond-copper (DBC) substrate and electrically connected through two leads to a curve tracer and a surge current test board. Fig. 1(c) shows a double-side-cooled Ga_2O_3 package ready for test.

It should be noted that the cooling structure in this work is discussed in the context of a 10-ms transient instead of the steady state. The thickness of Ag plate (1 mm) is designed to ensure that the heat diffusion is confined in the plate during the 10-ms transient (validated in the simulation in Section III, see Fig. 3). The bottom solder and DBC in both packages as well as the top wire bond in the double-side package do not contribute to the heat dissipation during the 10-ms transient.

Fig. 1(d) and (e) show the surge-current test circuit and the prototype, respectively. The test circuit is similar to the one reported in [15]. A 10-ms-wide half-sinusoidal current waveform was produced by a resonance circuit (a 2.2-mH inductor and a 4.7-mF capacitor). SiC MOSFETs were used as the control switches. The peak surge current (I_{peak}) was stepped up by increasing the power supply voltage. The device voltage was monitored by a differential probe, and the current was sensed by a 0.1-Ω coaxial current shunt (SSDN series). After each single-pulse surge-current test, the device was measured on the curve tracer to identify any possible degradation.

III. Experimental Results and Physical Analysis

Fig. 1(f) and (g) show the temperature-dependent I-V curves of the packaged large-area Ga_2O_3 SBDs in the linear region and the subthreshold region, respectively. The I-V characteristics of the SBDs in both packages are almost identical. The current on/off ratio is ~10^9 at 33 °C and maintains ~10^7 at 153 °C, suggesting the good thermal stability of the Schottky contact. The turn-on voltage is ~0.85 V at 33 °C and decreases to ~0.65 V at 153 °C. The current reaches 13 A (144 A/cm^2) at a forward voltage of 2 V. The temperature dependence of on-resistance (R_{on}) can be fitted by a power law with a temperature coefficient (α) of 0.73. This α is much smaller than the one reported for SiC SBDs (2.95 [19]), suggesting the superior thermal stability of Ga_2O_3 SBDs. This could be attributed to the small temperature dependence of mobility in Ga_2O_3 [12] and the increased donor ionization at high temperatures [16].

The breakdown voltage (BV) of the fabricated Ga_2O_3 SBDs was measured to be ~700 V, similar to the one reported in [16] using a similar edge termination, regardless of the packaging structures. Note that this BV is limited by the edge termination and has not reached the material limit. If suitable termination were used, e.g., the one reported in [3] that produces an average junction field of 3.4 MV/cm, the BV of the chip used in this work could reach 1600 V.

Fig. 2(a) and (b) show the current/voltage waveforms in a set of surge current tests with increased I_{peak} for the Ga_2O_3 SBDs with both package structures. The Ga_2O_3 SBD with the bottom-side-cooling package was found to fail in the surge test with an I_{peak} of 39 A. The failure I_{peak} is much higher (70 A) in the double-side-cooled SBD. Fig. 2(c) and (d) show the surge I-V loops of the SBDs with both types of packages. Both I-V loops are clockwise, due to the increased R_{on} at higher T_j, and the loop area is correlated to the R_{on} (and T_j) increase in the surge test. With a similar I_{peak} (e.g., 30 A), the loop area of the double-side-cooled SBD is smaller than that of the bottom-side-cooled SBD, suggesting a smaller T_j increase. In addition, the last safe-withstand I-V loop of the double-side-cooled Ga_2O_3 SBD (I_{peak} ~ 68 A) shows a larger area than that of the bottom-side-cooled SBD (I_{peak} ~ 37.5 A), implying that the double-side-cooled SBD can sustain a higher T_j. Fig. 2(e) shows the transfer characteristics of the double-side-cooled SBD after each surge test with increased I_{peak}. Almost no device degradation is shown with I_{peak} up to 60 A. At 68 A I_{peak}, higher leakage current is present, suggesting the degradation in the Schottky contact.

TABLE I.
KEY MODELS IN THE ELECTROTHERMAL SIMULATION

Parameter	Models and key parameters
Ga_2O_3 electron mobility (cm^{2}V^{-1}s^{-1})	Klaassen's Unified Low-Field Mobility Model mumaxn.kla = 120 (drift region) /30 (substrate)
Ga_2O_3 k_T (Wcm^{-1}K^{-1})	$k(T_L) = 0.1\times (T_L/300)^{-0.95}$ (T_L: lattice temp.)
Ga_2O_3 heat capacity (JK^{-1})	$C(T_L) = 0.2038 + 0.00174\times T_L - 1.459\times 10^{-6}\times T_L^2$
Nano-Ag k_T (Wcm^{-1}K^{-1})	$k(T_L) = 1\times (T_L/300)^{-0.14}$
Nano-Ag thermal contact resistance	0.087 K·cm^2/W
Thermal boundary condition	0.2 W/(cm^2·K) heat transfer coefficients at the exterior top/bottom surfaces

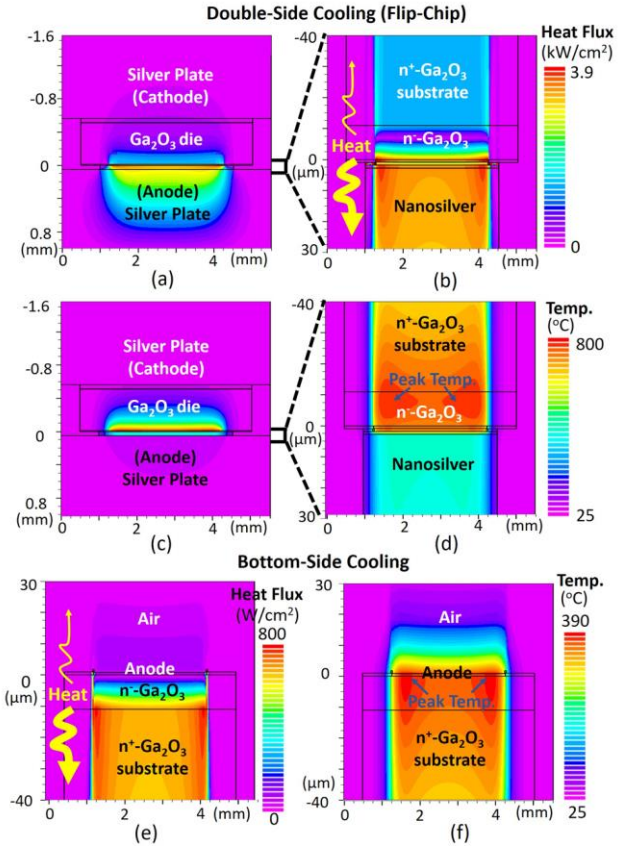


Fig. 3. Simulated heat flux contour in the (a) entire packaged device and (b) device junction region, and simulated temperature distributions in the (c) entire device and (d) junction region, in a double-side-cooled Ga_2O_3 SBD at the peak T_j transient in the surge current test with 68 A T_{peak}. Simulated (e) heat flux contour and (f) temperature contour in the junction region of the bottom-side-cooled Ga_2O_3 SBD at the peak T_j transient in the surge current test with 37.5 A T_{peak}.

To understand the electrothermal dynamics within the device structure, mixed-mode electrothermal TCAD simulations were performed in Silvaco Atlas, which solves the self-consistent electrothermal device models [20] in a circuit arrangement consistent with that shown in Fig. 1(d). Temperature-dependent k_T, heat capacity, and electron mobility models were employed for Ga_2O_3 and nanosilver (Table I). A good agreement between the simulation and experiment was achieved in static I-V curves and the surge I-V loops (Fig. 2(f)-(g)).

Fig. 2(h) shows the simulated T_j evolution at the Schottky contact region of the two types of SBDs in the surge current tests. In the test with a similar I_{peak}, the simulation validates a lower peak T_j in the double-side-cooled SBD. The simulated T_j reaches the peak value at the transient $t \approx 6$ ms, agreeing with the failure transients shown in Fig. 2(a) and (b). The simulation also verifies a smaller T_j in the bottom-side-cooled SBD at its critical I_{peak} (~ 37.5 A) as compared to the one in the double-side-cooled SBD (critical I_{peak} ~ 68 A).

Figs. 3(a)-(d) show the simulated distributions of heat flux and temperatures in the double-side-cooled SBD at the peak T_j transient in the surge current test with I_{peak} ~ 68 A. Fig. 3(e)-(f)

TABLE II
COMPARISON OF THE SURGE CURRENT CAPABILITY OF SIC AND GA_2O_3 SCHOTTKY BARRIER DIODES

Device	Rated Current (A)	Max Surge Current (A)	Max surge current over rated current
SiC SBD (CSD01060A)	4	20.3	5.1
SiC SBD (CSD02060A)	8	26.9	3.36
SiC SBD (CSD03060A)	11	31.8	2.89
Bottom-side-cooled Ga_2O_3 SBD	6.2	37.5	6.05
Double-side-cooled Ga_2O_3 SBD	9.2	68	7.4

show the simulated heat flux and temperature contours in the bottom-side-cooled SBD at the peak T_j transient in the surge current test with I_{peak} ~ 37.5 A. The heat flux distribution in the double-side-cooled SBD reveals that most heat is dissipated directly from the Schottky junction instead of through the Ga_2O_3 die. This explains the lower T_j in the double-side-cooled SBD as compared to that in the bottom-side-cooled SBD at a similar I_{peak}. As shown in Figs. 3(c) and (d), the simulated peak temperature is located within the Ga_2O_3 drift layer in the double-side-cooled SBD. In contrast, as shown in Fig. 3(f), the peak temperature is located at the Schottky junction in the bottom-side-cooled SBD. The double-side-cooling package moves the peak temperature from the Schottky contact region into the robust bulk Ga_2O_3, which allows the device to sustain a higher T_j before degradation of the Schottky contact.

Additionally, as shown in Figs. 3(d) and (f), the temperature distribution at the Schottky junction region is much less uniform in the bottom-side-cooled SBD compared to that in the double-side-cooled SBD. This temperature non-uniformity could be exacerbated by the wire bonding on the top of the anode in the bottom-side-cooled SBD, which often induces local current crowding and thermal runaway. This explains the lower T_j that bottom-side-cooled SBDs can sustain as compared to the one that double-side-cooled SBDs can. This mechanism is supported by the observation of burning traces near the wire bonds in the failed bottom-side-cooled SBDs.

IV. Benchmark, Discussion and Conclusion

An important device ruggedness metric for practical power applications is the ratio between the maximum I_{peak} in 10-ms surge current tests and the rated current. The rated currents of the bottom-side-cooled and double-side-cooled Ga_2O_3 SBDs were determined by the calibrated static electrothermal simulations when the T_j reaches 150 °C, being 6.2 A for the bottom-side-cooled device and 9.2 A for the double-side-colled device. For comparison, several commercial SiC SBDs with similar ratings (600-V voltage rating and 4~11 A current ratings) were tested in the same surge current test setup to identify their maximum surge currents. As shown in Table II, despite the low k_T of Ga_2O_3 (1/20 of SiC), the fabricated Ga_2O_3 SBDs, particularly the ones with double-side-cooling package, show comparable, or even superior surge current capabilities as compared to the similarly-rated commercial SiC SBDs.

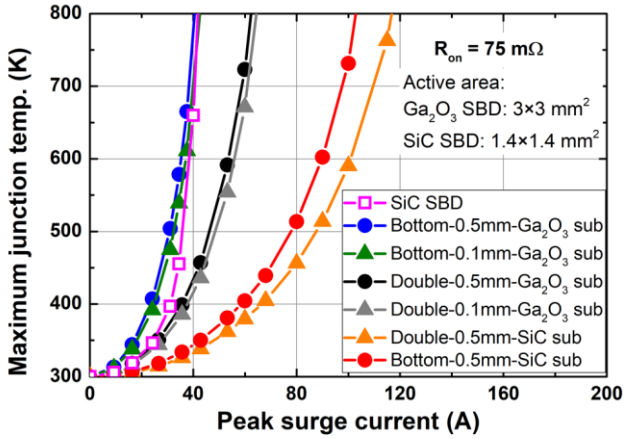


Fig. 4. Simulated max junction temperature as a function of peak surge current in 10-ms surge tests for the double-side-cooled and bottom-side-cooled Ga_2O_3 SBDs on the 0.5-mm-thick Ga_2O_3 substrate, 0.1-mm-thick Ga_2O_3 substrate, and 0.5-mm-thick SiC substrate. A thermal boundary resistance of 0.01 K/(W·cm²) was set at the Ga_2O_3/SiC bonding interface. Identical electrical conductivity was set for Ga_2O_3 and SiC substrates. The simulated SiC SBD has a 0.5-mm-thick substrate and a bottom-side-cooled package. Caughey-Thomas model was used for the SiC electron mobility.

Commercial SiC SBDs usually have bipolar p-n junctions that enhance the device ruggedness. Without p-type doping in Ga_2O_3, the superior surge current capabilities of Ga_2O_3 SBDs can be attributed to two mechanisms: first, the inherently smaller α in Ga_2O_3 devices allows for a small conduction loss increase with increased T_j and less risks for thermal runaway; second, the double-side-cooling package obviates the heat extraction via the low-k_T Ga_2O_3 chip and moves the peak temperature from the Schottky contact into the bulk Ga_2O_3.

To further understand the design space of the surge current capabilities of Ga_2O_3 devices, two additional die-level thermal management approaches were considered: thinning of the Ga_2O_3 substrate, and bonding Ga_2O_3 device layers to a SiC wafer [21]. Using the calibrated simulation models, Fig. 4 shows the simulated peak T_j as a function of surge I_{peak} for the different Ga_2O_3 device structures. A similarly-rated SiC SBD with identical substrate thickness was also simulated as a reference. In Ga_2O_3 devices, the substrate thinning provides little improvement in the surge current capabilities when compared to the use of junction cooling, since most of the heat is directly extracted from the junction. Whereas, if low-k_T SiC substrate is used in Ga_2O_3 devices, the heat extraction through the bulk chip can be improved significantly. Hence, the surge current capabilities can be further improved in the double-side-cooled device as compared to the bottom-side-cooled one.

In summary, this work presents the first experimental demonstration of large-area vertical Ga_2O_3 SBDs with different die-level cooling packages, and for the first time, reports the surge current capabilities of these packaged Ga_2O_3 devices. Despite the low k_T of Ga_2O_3, Ga_2O_3 SBDs packaged in a double-side-cooling scheme show comparable or even superior surge current capabilities when compared to SiC SBDs. These results remove the key concerns regarding the electrothermal ruggedness of Ga_2O_3 devices and demonstrate the significance of die-level thermal management for Ga_2O_3 electronics.

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